cntd F2

a NOR circuit having an input of said chip active enable signal and having input thereto [an inversion of] said inverted self refresh enable signal; and

a[n] NAND circuit having input thereto said output signal of said substrate voltage level detector and an output signal of said NOR circuit, said NAND circuit controlling said first PMOS transistor.

Kindly add the following new claim:

F3

--8. (New) A substrate bias generator according to claim 1, wherein said substrate voltage level detector includes:

a first MOS transistor having one source/drain terminal connected to a power supply, said first MOS transistor being operated in response to an output of said controller; and

a second MOS transistor having one source/drain terminal connected to the other source/drain terminal of said first MOS transistor and the other source/drain terminal connected to a ground supply, and having a gate connected to said substrate voltage.--

REMARKS

Entry and consideration of the foregoing amendment and following remarks are respectfully requested. By this amendment, the specification has been editorially amended, claims 1-4 and 7 have been amended, and claim 8 has been added. Upon entry of this amendment, claims 1-5 and 7-8 will be pending in the application.

1. Objections to the Disclosure

In the Office Action mailed April 5, 1996 in the parent application, the disclosure was objected to because a sentence in page 6 began with a non-capitalized word. It has been corrected.

2. Claim Rejections Under 35 U.S.C. § 112 (Second Paragraph)

In the parent application, claims 1-5 and 7 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite.

The portions of claim 1 related to the "channel" and the first MOS transistor, noted by the Examiner in the rejection, have been cancelled and incorporated into new dependent claim 8. Although the use of the term "channel" to describe the induced channel of a MOS transistor is believed appropriate, this language in new claim 8 and original claim 4 has been amended. These claims now recite that the MOS transistors have source/drain terminals connected to defined elements. Moreover, the corresponding language in claim 8 relating to the operation of the first MOS transistor, formerly contained in claim 1, has been replaced to define the first MOS transistor as being operated in response to an output of the controller.

The Examiner's suggested changes to claim 3 relating to the input of the chip enable signal have been proposed. Claims 3 and 7 have also been amended to further recite an inverter which inverts the self refresh enable signal to address the Examiner's concerns.

In view of the amendments to the claims and the foregoing remarks, the § 112 (second paragraph) rejection of the claims should be withdrawn.

3. Claim Rejections Under 35 U.S.C. §103

Claims 1 and 4-5 were rejected in the parent application under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,329,168 to Sugibayashi et al. ("Sugibayashi"). Applicant respectfully traverses this rejection in view of the amendments to the claims and the following remarks.

In accordance with an object of the present invention to provide a substrate bias generator which reduces current consumption during a self refresh mode, claim 1 (and similarly in claim 4) recites a controller which controls an operation of a substrate voltage level detector such that:

> said substrate voltage level detector is <u>not operative to drive said oscillator in the standby state of the self-refresh mode</u> of said semiconductor memory device and when said detected substrate voltage level is a desired level.

By virtue of this patentable feature, current consumption by the substrate voltage level detector, and accordingly, the substrate bias generator, is markedly reduced during the self-refresh mode.

Sugibayashi does not suggest this feature. Sugibayashi merely teaches a substrate bias system which receives power either from an external power voltage or an internal power voltage. Nowhere does Sugibayashi contemplate the problem of current consumption in the standby state of the self-refresh mode, much less the Applicant's solution whereby a substrate voltage level detector is rendered inoperative during this state and when the detected substrate voltage level is a desired level.

For the foregoing reasons, amended independent claims 1 and 4 patentably define over the cited prior art. Accordingly, the § 103 rejection of these claims, and claim 5 which depends from claim 4, should be withdrawn.

4. Allowable Subject Matter

The Examiner indicated that claims 2 and 3 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 (second paragraph). Since these claims have been amended as required, they should be allowed.

5. New Claim

Claim 8 contains subject matter cancelled from claim 1 and is added so that claims of varying scope are presented.

6. Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

CUSHMAN DARBY & CUSHMAN
Intellectual Property Group of
PILLSBURY MADISON & SUTRO LLP

By John P. Moran 30,906
David A. Jakopin
Reg. No. 32,995
Tel. No.: (202) 861-3739
Fax No.: (202) 822-0944

DAJ/MJD/jv
1100 New York Avenue, N.W.
Ninth Floor, East Tower
Washington, D.C. 20005-3918
(202) 861-3000